REMARKS

Upon entry of this amendment, claims 1 through 17 will be in the application, with claims 1 and 9 having been amended. Claims 1 and 9 are the independent claims herein. No new matter has been added. Entry of this amendment and further examination are respectfully requested.

Claims Rejections

Claims 1 through 3 and 5 through 11 are rejected under 35 USC § 103(a) as being unpatentable over Japanese patent JP 11219825 ("JP'825") in view of U.S. Patent No. 6,759,937 ("Kyriazidou"). Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 1

Amended independent claim 1 describes a device comprising a first layer of a multilayer substrate, a second layer of a multilayer substrate, a first section of an inductor, a second section of the inductor, a shielding plane, a first dielectric layer, and a second dielectric layer. The first layer has a first portion and a second portion. The second layer has a third portion and a fourth portion. The first section of an inductor is disposed in the second portion of the first layer and the second section of the inductor is disposed in the third portion of the second layer. The second section of the inductor is coupled at a plurality of locations to the first section of the inductor. The shielding plane is disposed between the first layer and the second layer. The first dielectric layer is disposed between the first layer of a multilayer substrate and the shielding plane and the second dielectric layer is disposed between the first layer of a multilayer substrate and the shielding plane. Moreover, a vector normal to the first section of an inductor does not intersect any other section of the inductor.

FIG. 1 of the present application reflects one embodiment of the foregoing features. Attachment A is a marked-up version of FIG. 1 showing a device 1 comprising a first layer 20 of a multilayer substrate, a second layer 30 of the multilayer substrate, a first section 12 of an inductor 10, a second section 16 of the inductor, a shielding plane 40, a first dielectric layer 50, and a second dielectric layer 60. The first layer 20 has a first portion 71 and a second portion 72.

The second layer 30 has a third portion 73 and a fourth portion 74. The first section 12 of an inductor 10 is disposed in the second portion 72 of the first layer 20 and the second section 16 of the inductor 10 is disposed in the third portion 73 of the second layer 30. Moreover, a vector 70 normal to the first section 12 of the inductor 10 does not intersect any other section of the inductor 10.

The art of record is not seen to disclose or suggest the above-mentioned features of amended independent claim 1. In particular, the art of record is not seen to disclose or to suggest a vector normal to a first section of an inductor that does not intersect any other section of the inductor.

As stated in the previous response, JP'825 illustrates a surface mounted transformer that includes dielectric sheets 7a and 7b and spiral inductors L1 and L2. Spiral inductor L1 is located on an upper surface of dielectric sheet 7a and spiral inductor L2 is located on an upper surface of dielectric sheet 7b. An inner most end of inductor L1 is connected to connection sheet 2 and an outer most end of inductor L1 is connected to the outer most end of inductor L2. Inductors L1 and L2 are not connected at any other points.

Kyriazidou describes a multi-layer inductor. As illustrated in FIG 3 and FIG 4, Kyriazidou discloses a first partial winding 12 on a first layer 14 and a fourth partial winding 22 on a second layer 20. At FIG 4, the fourth partial winding 22 is shown as located below the first partial winding 12. Thus, a vector normal to the first partial winding 12 and intersecting the first partial winding 12 would also intersect the fourth partial winding 22.

Accordingly, nowhere can Kyriazidou possibly be seen to disclose or to suggest a vector normal to a first section of an inductor that does not intersect any other section of the inductor.

In view of at least the foregoing, amended independent claim 1 is believed to be in condition for allowance. Claims 2, 3, and 5 through 8 depend from amended independent claim 1 and are therefore also believed to be in condition for allowance.

Amended independent claim 9 describes a method to fabricate an inductor in a first and second layer of a multilayer substrate, in which, a vector normal to a first section of an inductor

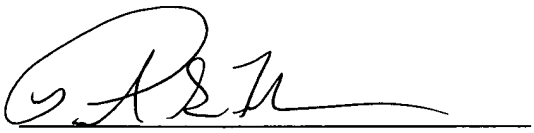
does not intersect any other section of the inductor. In view of at least the foregoing, amended independent claim 9 and its related dependent claims are believed to be in condition for allowance.

CONCLUSION

The outstanding Office Action presents a number of characterizations regarding the applied references, some of which are not directly addressed by this response. Applicants do not necessarily agree with the characterizations and reserve the right to further discuss those characterizations.

For at least the reasons given above, it is submitted that the entire application is in condition for allowance and such action is respectfully requested at the Examiner's earliest convenience. Alternatively, if there remains any question regarding the present application or any of the cited references, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-4982.

Respectfully submitted,



May 23, 2006
Date

Richard S. Finkelstein
Registration No. 56,534
Buckley, Maschoff & Talwalkar LLC
Attorneys for Intel Corporation
Five Elm Street
New Canaan, CT 06840
(203) 972-4982

Attachment: Attachment A

ATTACHMENT A